Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A microcontroller with expandable memory banks, the microcontroller comprising:

a microprocessor;

a plurality of memory banks connected to the microprocessor for storing data, programs;

a memory bank control circuit connected to the microprocessor for asserting a signal during the processing of an interrupt event; and

a multiplexer for connecting the microprocessor with the plurality of memory banks, the multiplexer comprising:

a first input connected to an output of the microprocessor for bank switching during the normal operation;

a second input connected to a predetermined value corresponding to the memory bank storing the interrupt service routines; and

a selecting port connected to an output of the memory bank control circuit for selecting whether to output an page selection signal from the output of the microprocessor or an predetermined page selection signal,

wherein the microprocessor can access data stored in the memory bank storing the interrupt service routines

when the interrupt occurs.

[c2] 2.The microcontroller of claim 1 wherein the microprocessor is an MCS series microprocessor.

[c3] 3.The microcontroller of claim 1 wherein the plurality of memory banks are expandable and have a storage space larger than a command addressing capacity of the microcontroller.

[c4] 4.The microcontroller of claim 1 wherein the multiplexer further comprises extra input for a different predetermined page selection signal corresponding to the memory bank storing different interrupt service routines.

[c5] 5.The microcontroller of claim 1 wherein the memory bank control circuit generates a selection signal according to one of different interrupt sources.

[c6] 6.The microcontroller of claim 1 wherein each memory bank comprises a common area that does not comprise the interrupt service routines.

[c7] 7. The microcontroller of claim 1 wherein any program called by the interrupt service routine and the interrupt service routine are stored in the same memory bank.

[c8] 8. A method for accessing a memory connected to a microprocessor, wherein the memory comprises a plurality

of memory banks, the method comprising:

(a) storing interrupt service routines in one of the plurality of memory banks;

(b) when an interrupt of the microprocessor does not occur, selecting and accessing a memory bank according to a page selection signal output by the microprocessor; and

(c) when an interrupt of the microprocessor occurs, selecting and accessing the memory bank storing the interrupt service routines according to a predetermined page selection signal.

[c9] 9. The method of claim 8 wherein the microprocessor is an MCS series microprocessor.

[c10] 10. The method of claim 8 further comprises storing a common area not comprising the interrupt service routines in each memory bank.

[c11] 11. The method of claim 8 further comprises storing a program called by the interrupt service routines in the same memory bank with the interrupt service routines.